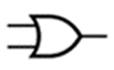
******Porta Lógica - Logic Gate OR ou OU ou +**

**Porta NOT ou INVERTER (inversor)**

**Porta Lógica - Logic Gate AND ou E ou \***

**Desafio 4.5 – Tendo em conta a expressão + B+ .**

a) Calcular o nº de saídas possíveis.

b) Preencher a tabela de verdade.

c) Desenhar o circuito no logisim.

d) Desenhar o diagrama temporal.

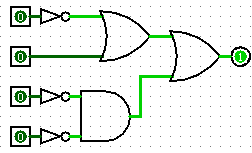
e) Conclusão.

**Resolução**

a) Calcular o nº de saídas possíveis. Resposta 24=\_\_16\_\_

b) Preencher a tabela de verdade

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Entradas | | | |  |  |  |  |  |
| A | B | C | D |  | **D’** |  | **.** | **+ B+ .** |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| 0 | 1 | 1 | 0 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 | 0 |
| 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |
| 1 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 | 0 | 1 | 0 | 0 | 1 |
| 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 |

b) Desenhar o circuito no logisim.

c) Desenhar o diagrama temporal.

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| A | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| B | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| C | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| D | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| S | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 |  |

f) Conclusão. A saída será 0, quando B=0 ou B e C =0 ou B e D =0