**Porta Lógica - Logic Gate AND ou E ou \***

**Porta NOT ou INVERTER (inversor)**

**Porta Lógica - Logic Gate NAND (Não E)**

**Desafio 5 – Tendo em conta a expressão** $\overbar{A}$ **.**$\overbar{B}$

**Desafio 5.1 – Tendo em conta a expressão**  $\overbar{A.B}$

a) Calcular o nº de saídas possíveis.

b) Preencher a tabela de verdade.

c) Desenhar o circuito no logisim.

d) Desenhar o diagrama temporal.

e) Conclusão.

**Resolução**

a) Calcular o nº de saídas possíveis. Resposta 22=\_4\_\_

b) Preencher as tabelas de verdade

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| 22=4 | Entradas |  | Saída$\overbar{A}$ **.**$\overbar{B}$ |
| **A** | **B** | $$\overbar{A}$$ | $$\overbar{B}$$ | **S** |
| 1 | 0 | 0 | 1 | 1 | 1 |
| 2 | 0 | 1 | 1 | 0 | 0 |
| 3 | 1 | 0 | 0 | 1 | 0 |
| 4 | 1 | 1 | 0 | 0 | 0 |

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| 22=4 | Entradas |  | Saída$$\overbar{A.B}$$ |
| **A** | **B** | **A.B** | **S** |
| 1 | 0 | 0 | 0 | 1 |
| 2 | 0 | 1 | 0 | 1 |
| 3 | 1 | 0 | 0 | 1 |
| 4 | 1 | 1 | 1 | 0 |

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b) Desenhar os circuitos no logisim.



c) Desenhar os diagramas temporais.

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|  |  |  |  |  |  |
| A | 0 | 0 | 1 | 1 |  |
|  |  |  |  |  |  |
| B | 0 | 1 | 0 | 1 |  |
|  |  |  |  |  |  |
|  |  |  |  |  |  |
| S | 1 | 0 | 0 | 0 |  |

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|  |  |  |  |  |  |
| A | 0 | 0 | 1 | 1 |  |
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| B | 0 | 1 | 0 | 1 |  |
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|  |  |  |  |  |  |
| S | 1 | 1 | 1 | 0 |  |

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f) Conclusão. Conclui-se que, negar as entradas de uma porta produz um resultado diferente ao de negar a saída de uma mesma porta.