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| **LATCH ou Flip-Flop RS assíncrono** |

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| --- | --- |
|  | A imagem representa um Flip-Flop com portas NANDR significa RESET e S significa SET, ou seja, R Desliga a saída e S Liga a saída. |
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| Símbolo  | Tabela de verdade |
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| **R** | **S** | **Q** | **Q’** | Estado |
| 0 | 0 | Qa (Q anterior) | Q’a (Q’ anterior) | Memória |
| 0 | 1 | 1 | 0 | Set |
| 1 | 0 | 0 | 1 | Reset |
| 1 | 1 | 0 | 0 | Erro lógico |

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Completa o diagrama temporal



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| **LATCH ou Flip-Flop RS síncrono** |

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| Circuito lógico | Descrição |
|  | A imagem representa um Flip-Flop com portas NANDR significa RESET e S significa SET, ou seja, R Desliga a saída e S Liga a saída.CLK significa Clock e permite habilitar ou desabilitar todo o circuito.Este circuito entra em memória quando R=0 e S=0 ou quando CLK=0  |

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| Símbolo |  | Tabela de verdade |
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| **Entradas** | **Saídas** | **Estado** |
| CLK | R | S | Q | Q’ |
| 0 | x | x | Qa | Qa’ | Mem. |
| 1 | 0 | 0 | Qa | Qa’ | Mem. |
| 1 | 0 | 1 | 1 | 0 | Set |
| 1 | 1 | 0 | 0 | 1 | Reset |
| 1 | 1 | 1 |  |  | Erro |

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Completa o diagrama temporal



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| **LATCH D síncrono** |

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| Circuito lógico  | Descrição |
|  | A imagem representa um Latch tipo D com portas NANDR significa RESET e S significa SET, ou seja, R Desliga a saída e S Liga a saída. D significa Dado ou *data.*CLK significa Clock e permite habilitar ou desabilitar todo o circuito.Este circuito entra em memória quando R=0 e S=0 ou quando CLK=0  |
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| Símbolo |  |  |
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| **Entradas** | **Saídas** | **Estado** |
| **CLK** | D | Q | Q’ |
| 0 | X | Qa | Qa’ | Mem. |
| 1 | 0 | 0 | 1 | Reset |
| 1 | 1 | 1 | 0 | Set |

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Completa o diagrama temporal

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| D |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| CLK |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Q | r | r | m | m | r | r | m | r | s | r | m | m | m | s | m | m | s | m | m | r |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Q’ |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
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| **Flip-Flop JK** |

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| Circuito lógico | Descrição |
|  | A imagem representa um Flip-Flop do tipo JK com portas NANDJ significa SET e K significa RESET, ou seja, K Desliga a saída Q e J Liga a saída Q. |
| CLK significa Clock e permite habilitar ou desabilitar todo o circuito.Este circuito entra em memória quando J=0 e K=0 ou quando CLK=0 Quando J=1 e K=1 o circuito entra em Toggle ou Inversão. |

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| Símbolo |  | Tabela de verdade |
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| **Entradas** | **Saídas** | **Estado** |
| CLK | J | K | Q | Q’ |
| 0 | x | x | Qa | Qa’ | Mem. |
| 1 | 0 | 0 | Qa | Qa’ | Mem. |
| 1 | 0 | 1 | 0 | 1 | Reset |
| 1 | 1 | 0 | 1 | 0 | Set |
| 1 | 1 | 1 | Qa’ | Qa | Inversão*toggle* |

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Completa o diagrama temporal



Completa o diagrama temporal

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| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| J | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| K | 0 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| CLK | 1 |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Q | 1 |  |  |  |  |  |  |  | T | T | T | T | T |  | T |  |
|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| Q’ | 0 |  |  |  |  |  |  |  | T | T | T | T | T |  | T |  |
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| **Flip-Flop JK ms** |

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| Circuito lógico | Descrição |
|  | A imagem representa um Flip-Flop do tipo JK MS (M= Master e S= Slave) com portas NANDJ significa SET e K significa RESET, ou seja, K Desliga a saída Q e J Liga a saída Q. |
| CLK significa Clock e permite habilitar o MASTER e Desabilitar o SLAVE ou Desabilitar o MASTER e Habilitar o Slave.Este circuito entra em memória quando J=0 e K=0 ou quando CLK=0 ou CLK=1Os FFjkMS funcionam na subida ou descida do Clok. Um FF que funciona pela borda de subida diz-se de transição positiva, um FF que funciona na borda de descida diz-se de transição negativa |

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| Símbolo | Tabela de verdade |
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| **Entradas** | **Saídas** | **Estado** |
| CLK | J | K | Q | Q’ |
| 0/1 | x | x | Qa | Qa’ | Mem. |
| ˄ | 0 | 0 | Qa | Qa’ | Mem. |
| ˄ | 0 | 1 | 0 | 1 | Reset |
| ˄ | 1 | 0 | 1 | 0 | Set |
| ˄ | 1 | 1 | Qa’ | Qa | Inversão*toggle* |

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Completa o diagrama temporal

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| J |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
| K |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
| CLK |  |  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
| Q |  |  | T |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |  |  |
| Q’ |  |  |  |  |  |  |  |  |  |

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| **Flip-Flop JK ms, com base em FF rs. FINAL** |

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| Tabela de verdade e mapa de Karnaugh |
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| **Entradas** | **Saídas** |
| Posição | J | K | Qa | s | r |
| 0 | 0 | 0 | 0 | 0 | 1 |
| 1 | 0 | 0 | 1 | 1 | 0 |
| 2 | 0 | 1 | 0 | 0 | 1 |
| 3 | 0 | 1 | 1 | 0 | 1 |
| 4 | 1 | 0 | 0 | 1 | 0 |
| 5 | 1 | 0 | 1 | 1 | 0 |
| 6 | 1 | 1 | 0 | 1 | 0 |
| 7 | 1 | 1 | 1 | 0 | 1 |

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| Expressões boleanas encontradas para S e R. S=K’Qa+JQa’R=S’ |

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| Completa o diagrama temporal |
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| Completa o diagrama temporal |
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| **Flip-Flop JK ms, com base em (FF rs) com CLEAR PRESET (CLR PR)** |
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| A imagem representa um Flip-Flop do tipo Flip-Flop JK ms, com base em (FF rs) com CLEAR PRESET (CLR PR) com portas NAND |

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| Tabela de verdade

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| --- | --- | --- |
| **Entradas** | **Saídas** | **Estado** |
| CLK | J | K | **PR’** | **CLR’** | Q | Q’ |   |  |  |
| x | x | x | 0 | 0 | 1 | 1 | Erro |
| x | x | x | 0 | 1 | 1 | 0 | Set |
| x | x | x | 1 | 0 | 0 | 1 | Reset |
| 0/1 | x | x | 1 | 1 | Qa | Qa’ | Mem. |
| ˄ | 0 | 0 | 1 | 1 | Qa | Qa’ | Mem. |
| ˄ | 0 | 1 | 1 | 1 | 0 | 1 | Reset |
| ˄ | 1 | 0 | 1 | 1 | 1 | 0 | Set |
| ˄ | 1 | 1 | 1 | 1 | Qa’ | Qa | Inversão*toggle* |

 | Clear = CLR faz RESET ao circuitoPreset = PR faz SET ao circuito |

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Completa o diagrama temporal

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